

## REMARKS

Claims 1, 5, 11 and 15 have been amended.

Applicant believes that this response addresses the Examiner's rejection and that any changes do not introduce new matter into the specification, limit the scope of the claims or result in any prosecution history estoppel.

### Claim Rejections – 35 U.S.C. §103

The Examiner rejected claims 1-20 under 35 USC 103 as being unpatentable over Easter (5,530,749) and Elgamal (5,657,390). Applicant respectfully disagrees with the Examiner's rejection. In particular, both Easter and Elgamal, alone or in communication, fail to teach or suggest "programming a re-configurable hardware block based upon the decrypted key to establish a unique hardware configuration, wherein the configuration is changed at regular intervals" as claimed or similarly claimed. As noted in the present application at page 2, line 25- page 3, line 3:

The present invention provides an inferred hardware assisted decryption (IHAD) electronic system 10 that utilizes a re-configurable hardware block in conjunction with a processor running a software decryption algorithm that determines the form of the hardware. The re-configurable feature of the IHAD allows the hardware to be changed at regular intervals, thus circumventing any attempts at compromising the hardware. For example, a new hardware configuration could be used everyday, or even every transaction. As a result, by the time the hardware is compromised, it is no longer being used. The speed benefits of a hardware only type of decryption can thus be realized without the limitations typically associated with hardware only solutions.

Easter and Elgamal, alone or in combination, fail to teach or suggest programming a re-configurable hardware block based upon the decrypted key to establish a unique hardware configuration, wherein the configuration is changed at regular intervals as claimed or similarly claimed. The Examiner relies on Easter at column 3, lines 65-column 4, line 10, which merely provides:

A customizable computer chip is used to selectively enable or configure features or functions of a multichip module. The invention can also be used on single chip modules wherein more than one process is contained within a single chip. In a first embodiment, each of the features, processors or functions is associated with a fusible array on the chip. A fusible array is a set of wires which are connected to ground at one end and available to logic at the other end. The array of wires is customized by cutting open a predetermined combination of wires. Each chip will have a unique combination of wires or in other words, a unique code. The fusible array can have two distinct portions.

Hardware can thus not be changed at regular intervals or even every transaction as in embodiments of the present invention. Rather, Easter just relies on comparing a key code to a secure code on the computer chip. An encrypted hardware code is not received and then decrypted.

### CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

No fees are required for additional claims. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: March 9, 2005

By

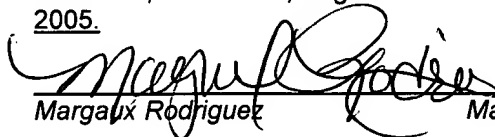


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### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on March 9, 2005.



Margaux Rodriguez

March 9, 2005